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PPLICATION NO.	F	ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/796,035		03/10/2004	Yoshihiro Maesaki	122.1583	122.1583 2112	
21171	7590	05/19/2005		EXAMINER		
STAAS & I SUITE 700	HALSEY	LLP	TANG, MINH NHUT			
	ORK AV	ENUE, N.W.		ART UNIT PAPER NUMBER		
WASHINGT	ON, DC	20005		2829		

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)	
		10/796,035	MAESAKI ET AL.	
	Office Action Summary	Examiner	Art Unit	
		Minh N. Tang	2829	
Dorind f	The MAILING DATE of this communication or Reply	n appears on the cover sheet w	vith the correspondence address	••
			AONTHIO EDOM	
THE - External after of the control	IORTENED STATUTORY PERIOD FOR R MAILING DATE OF THIS COMMUNICATION (INC.) And the provisions of 37 Clars (IV) (IV) (IV) (IV) (IV) (IV) (IV) (IV)	ON. FR 1.136(a). In no event, however, may a n. a reply within the statutory minimum of th eriod will apply and will expire SIX (6) MO statute, cause the application to become A	reply be timely filed irty (30) days will be considered timely. NTHS from the mailing date of this communi BANDONED (35 U.S.C. § 133).	cation.
Status		•		
1)⊠	Responsive to communication(s) filed on	22 February 2005.		
2a)⊠	•	This action is non-final.		
3)	Since this application is in condition for all	owance except for formal ma	tters, prosecution as to the meri	its is
	closed in accordance with the practice und	der <i>Ex parte Quayle</i> , 1935 C.	D. 11, 453 O.G. 213.	
Disposit	tion of Claims			
4) 又	Claim(s) 3-5 is/are pending in the applicat	ion.		
,	4a) Of the above claim(s) is/are with			
5)⊠	Claim(s) <u>5</u> is/are allowed.			
	Claim(s) <u>3</u> is/are rejected.		•	
	Claim(s) 4 is/are objected to.		•	
	Claim(s) are subject to restriction a	nd/or election requirement.	•	
Applica	tion Papers			
9)□	The specification is objected to by the Exa	miner.		
, —	The drawing(s) filed on <u>3/10/2004 & 2/22/2</u>		or b)∏ objected to by the Exami	iner.
,	Applicant may not request that any objection to			
	Replacement drawing sheet(s) including the co			121(d).
11)	The oath or declaration is objected to by the			
Priority	under 35 U.S.C. § 119			
_	Acknowledgment is made of a claim for for	reign priority under 35 U.S.C.	8 119(a)-(d) or (f)	
-	Acknowledgment is made of a claim for ion ⊠ All b)		3 113(d)-(d) 51 (i).	
	2. Certified copies of the priority documents		Application No	
	3. Copies of the certified copies of the			е
	application from the International B	ureau (PCT Rule 17.2(a)).		
*	See the attached detailed Office action for	a list of the certified copies no	ot received.	
Attachme	nt(s)	_		
	ice of References Cited (PTO-892)	•	y Summary (PTO-413) o(s)/Mail Date	
3) 🔲 Info	ice of Draftsperson's Patent Drawing Review (PTO-94 rmation Disclosure Statement(s) (PTO-1449 or PTO/S er No(s)/Mail Date	~/	Informal Patent Application (PTO-152)	
		,		

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DETAILED ACTION

Drawings

1. The drawings (Figs. 3, 5-6) were received on February 22, 2005. These drawings are approved.

Specification

2. The amendment to the specification filed on February 22, 2005 has been entered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 4. Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by Nakata et al. (U.S.P. 5,825,193).

As to claim 3, Nakata et al. disclose, in Fig. 1, a dynamic burn-in apparatus for a semiconductor device (11), wherein a signal output from a signal generator (i.e., a device for outputting an external signal applied at the external input terminal 15, hereinafter generator) is provided to a semiconductor device to be tested (11) in the burn-in tank (not shown), comprising: a converter (13) that is added at the output of the signal generator (generator) and located outside of the semiconductor device (11), wherein the frequency (i.e., 12.5 MHz) of the signal output (i.e., external signal) from the signal generator (generator) is increased (see column 4, lines 32-38) by the converter

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(13) and the signal output (i.e., reference signal) from the converter (13) is provided to the semiconductor device (11).

Allowable Subject Matter

- 5. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 6. Claim 5 is allowed over the art of record.
- 7. It is noted that if claim 4 is going to amend as noted in paragraph 5 above, then Applicant is advised that should claim 5 be allowable, claim 4 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Response to Arguments

8. Applicant's arguments filed on February 22, 2005 have been fully considered but they are not persuasive.

Applicants, in the Remarks page 9, filed on February 22, 2005, asserted that

Nakata et al. discloses that the frequency converter (13) is formed on the

semiconductor substrate (85) having a plurality of semiconductor integrated circuits, and

Nakata et al. does not disclose a converter that is added at the output of the signal

generator and located outside of the semiconductor device. The Examiner agrees that

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the frequency converter (13), the self-test circuit (12), the semiconductor device to be tested (11) are all formed on the semiconductor substrate (85), or in other word, the semiconductor substrate (85) supports the frequency converter (13), the self-test circuit (12), the semiconductor device to be tested (11); however, the Examiner respectfully disagrees that Nakata does not disclose a converter that is added at the output of the signal generator and located outside of the semiconductor device since the semiconductor device as recited in Applicants' claim 3 is a semiconductor device to be tested, therefore, it is believed that Nakata et al., as shown in Fig. 1, does disclose the converter (13) that is added at the output of the signal generator (i.e., a device for outputting an external signal applied at the external input terminal 15) and located outside of the semiconductor device to be tested (11).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Communication

10. Any inquiry concerning this or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor R. Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MINH NHUT TANG PRIMARY EXAMINER

5/03/05